REMARKS

The examiner has requested that the cross reference related to the application appearing on page 1, lines 4-7, of the specification must be updated with the relevant status. Attorney for applicants in a telephone conversation advised the examiner that the application was already identified with its serial number, filing date and description and that the status had not changed, i.e. no patent had yet issued. The examiner accepted this explanation and no amendment to the specification is, therefore, required.

The examiner has rejected claims 1-18 under 35 U.S.C. 103(a) as being unpatentable over Laurenti et al, U.S. Patent 6,658,578, hereinafter Laurenti et al, in view of Koga, U.S. Patent 5,530,904, hereinafter Koga. This rejection is not thought to be well taken especially in view of incorporation of the limitations of claim 4 in claim 1, the amendment of claim 7 to depend from claim 1 rather than canceled claim 4, and the amendments to claims 10 and 12.

Claims 1, 10 and 12, the only independent claims in the application, have been amended to confirm that the system is a communication system, and the time division multiplexer is used in conjunction with the buffers to output the data in the same order it was inputted. This is not shown or taught by any reasonable combination of Laurenti et al and Koga.

First, the Laurenti et al patent is a good example of the prior art which is referred to in the present application at page 1, line 13, through page 3, line 7:

> The use of parallel processing generically called multiprocessing is well known in data processing technology. In conventional data processing a plurality of processors are constrained to process subportions of a partitioned task and/or individual tasks in a set of tasks. The prior art abounds with multiprocessor patents, examples of which include:

U.S. Patent 4,718,006
U.S. Patent 5,021,945
U.S. Patent 5,327,419 and
U.S. Patent 5,692,119.

Even though multiprocessing systems are well known and used in data processing their use in communications technology is somewhat limited.

In this technology several problems have to be overcome if the system is to function satisfactorily. Among the many problems is that of sequencing. In particular, the sequence of data at the output of the system should be the same as when the data was received at the input.

The proper sequencing of data is particularly difficult in communications technology in which the data is delivered in units called a frame or packet which can be of different lengths.

Because of the difference in frame length, among other things, a processor could complete processing a short frame in less time than is required to process a long frame. As a consequence the processed short frame would be available at the output of the system before the processed long frame even though the sequence at the input was long frame followed by short frame.

To maintain the sequence the prior art uses complicated circuits to keep track of the sequence at delivery and at the output organizes the processed frames in the same order in which the frames were delivered at the input of the system. These circuits are costly and increase the cost of the system. In addition, additional silicon space is required to implement the circuits. In most designs silicon space is a scarce commodity and should be preserved whenever possible.

Another problem is throughput. In most communications networks data is received from a network operating at a particular data rate process by a receiving system and returned to the network. Usually, the processing rate of the receiving system is much slower than the data rate of the network. The discrepancy between data rates results in a bottleneck within the receiving system. In some applications the bottleneck is a negative that cannot be tolerated. As a consequence there is a need to provide receiving systems with throughput matching that of the network to which the receiving systems are connected.

Thus, the base reference is nothing more than the acknowledged prior art, except it does not use the term "network processor", which network processor is defined and described in U.S. Patent No. 6,769,033 B1. And the Koga patent, while teaching a time division multiplexor

(TDM), does not teach or suggest how a TDM could be used in conjunction with buffers to assure that data frames are outputted in the same order that they are inputted. As indicated in the foregoing quoted passage from the application, the extra circuitry and silicon space have been a problem in using multiprocessing in communications where the output must be in the same order as the input. It is the applicants who have shown how to use a TDM to assure such an output. This is not taught or suggested by either Laurenti et al, Koga, or any reasonable combination thereof. While Koga does suggest the use of a TDM, he in no way suggests that it could be used in combination with buffers to assure that the data is outputted in the same order that it is inputted. In fact, at the location cited by the examiner at column 3, the TDM is an alternate to arbitration, and arbitration certainly *does not* sequence the "data out" to match the order of "data in". Thus, it is submitted that there is no teaching in Koga that could suggest the combination with Laurenti et al to achieve the results claimed by applicants.

In rejecting claims under 35 U.S.C. §103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1986). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp.,

732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir.1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Since there is no teaching of sequencing the order of "data out" with the order that "data in" is received in any reference, there can be no teaching of such. Thus, independent claims 1, 10 and 12 are clearly allowable. Claims 2-9, 11, and 13-18 are dependent, either directly or indirectly, on claims 1, 10 and 12, respectively, and, for the same reasons, are believed to be allowable.

Moreover, claims 7-9 require certain properties of the TDM to achieve results which are neither taught nor suggested by Laurenti et al or Koga and, for these additional reasons, are believed to be allowable.

In view of the above, it is believed that each of the claims now in the application is distinguishable, one from the other and over the prior art. Therefore, reconsideration, and allowance of the claims is respectfully requested.

Respectfully submitted,

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